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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A digital to analog converter comprising a first current source (3) connected to a plurality of common lines (20,21) and to a first node (23,[[2]]36), wherein said first node (23,[[2]]36) forms an output of the digital to analog converter via a respective switch (35, 38, 46) whose state is controlled in accordance with a first applied digital signal (28,31) to be converted, the digital to analog converter further comprising a second current source (30) which is associated with said first current source (3), wherein said second current source (30) is connected to at least one of said common lines (20[[;]],21) and to a second node (26,37) via a respective second switch (39) whose state is controlled in accordance with a second applied digital signal (29,32), characterized in that second applied digital signal (29,32) causes said second respective switch (39) to change state such that influences on at least said one of said common lines (20[[;]],21) caused by said first and second switches (38,39) switching are periodic.
2. (original) A digital to analog converter according to claim 1, wherein said first signal (28,31) comprises a plurality of signal components (t1-t6) each having a duration substantially equal to one or more clock cycles, and wherein said second signal (29,32) is derived from said first signal (28,31) so that, during data conversion, during any one clock cycle either said first current source (3) or said associated second current source (30) is caused to switch.
3. (original) A digital to analog converter according to claim 1, further comprising a power supply (9) to which said first current source (3) and said second current source are connected (30).

4. (original) A digital to analog converter according to claim 1, wherein said first current source (3) is disposed adjacent to said second associated current source (30).
5. (original) A digital to analog converter according to claim 1, wherein said first and second digital signals (31,32) are carried on first and second digital input lines (28,29), respectively, wherein said first digital input line (28) is connected to said first switch (38) and said second digital input line (29) is connected to said second switch (39), wherein said first and second digital input lines (28,29) are arranged in parallel.
6. (original) A digital to analog converter according to claim 1, wherein said second digital signal (32) is generated by a signal generating means (10) comprising a circuit for identifying clock cycles in said first digital signal (31) in which, when applied to said first switch (38), a signal component causes said first current source (3) to switch, and for generating in response to the identification, a second digital signal (32) including a signal component which, when applied to said second switch (39), causes said second current source (30) to switch, in those clock cycles in which no such component is identified in said first digital signal (31), so that, during conversion, in any one clock cycle, either said first or said second current source (3,30) is caused to switch.
7. (currently amended) A digital to analog converter according to claim 1, wherein [[the]]output loads associated with first and second nodes (23,36,26,37) are substantially matched.
8. (original) A digital to analog converter according to claim 1, comprising a plurality of first current sources (3,5,7), each of which is associated with one of a plurality of second current sources (30,50,70), wherein each of said plurality of first and second current sources (3,30,5,50,7,70) is provided with a respective switch (39).
9. (currently amended) A method of converting a digital signal to an analog signal comprising the steps of:

providing a first current source (3),

connecting said first current source (3) to a plurality of common lines (20,21) and to a first node (23,[[2]]36), wherein said first node (23,[[2]]36) forms an output of the digital to analog converter via a plurality of respective switches (38) whose states are controlled in accordance with a first applied digital signal (28,31) to be converted,

further providing a second current source (30) which is associated with said first current source (3), connecting said second current source (30) to at least one of said common lines (20[[;]],21) and to a second node (26,37) via a respective second current switch (39) whose state is controlled in accordance with a second applied digital signal (29,32) characterized by applying said second digital signal (29,32) to said second respective switch (39) causing said respective second switch (39) to change state such that influences on at least said one of said common lines (20[[;]],21) caused by said first and second switches (38,39) switching are periodic.

10. (new) A digital to analog converter according to claim 1 wherein said second current source (30) is identical to said first current source (3).
11. (new) A digital to analog converter according to claim 7 wherein said output loads are components that register an output signal and put a load on the output nodes of the digital to analog converter.
12. (new) A digital to analog converter according to claim 7 wherein said output loads are a cable line.
13. (new) A digital to analog converter according to claim 7 wherein said output loads are an antenna.